WHAT IS CLAIMED IS:

1. A semiconductor apparatus comprising at least one double poly bipolar transistor and at least one double poly metal oxide semiconductor (MOS) transistor.

2. The semiconductor apparatus as set forth in Claim 1 wherein said at least one double poly bipolar transistor and said at least one double poly metal oxide semiconductor (MOS) transistor comprise a substrate and a first layer of polysilicon (Poly1) material wherein:

said first layer of polysilicon (Poly1) material in said at least one double poly bipolar transistor is doped with impurity ions to form an extrinsic base; and

said first layer of polysilicon (Poly1) material in said at least one double poly MOS transistor is simultaneously doped with impurity ions to form an MOS transistor gate.

3. The semiconductor apparatus as set forth in Claim 2 wherein said at least one double poly bipolar transistor is a PNP transistor and wherein said at least one double poly MOS transistor is an NMOS transistor.

4. The semiconductor apparatus as set forth in Claim 2 wherein said at least one double poly bipolar transistor is an NPN transistor and wherein said at least one double poly MOS transistor is a PMOS transistor.

5. The semiconductor apparatus as set forth in Claim 2 wherein said at least one double poly bipolar transistor is a PNP transistor and wherein said at least one double poly MOS transistor is a PMOS transistor.

6. The semiconductor apparatus as set forth in Claim 2 wherein said at least one double poly bipolar transistor is an NPN transistor and wherein said at least one double poly MOS transistor is an NMOS transistor.

7. The semiconductor apparatus as set forth in Claim 2 wherein:

said substrate is implanted with impurity ions to form an intrinsic base in said at least one double poly bipolar transistor; and

said substrate is simultaneously implanted with impurity ions to form a lightly doped drain in said at least one double poly MOS transistor.

8. The semiconductor apparatus as set forth in Claim 7 wherein said lightly doped drain in said at least one double poly MOS transistor is self aligned.

9. The semiconductor apparatus as set forth in Claim 7 wherein said at least one double poly bipolar transistor is a PNP transistor and wherein said at least one double poly MOS transistor is an NMOS transistor.

10. The semiconductor apparatus as set forth in Claim 7 wherein said at least one double poly bipolar transistor is an NPN transistor and wherein said at least one double poly MOS transistor is a PMOS transistor.

11. The semiconductor apparatus as set forth in Claim 7 wherein said at least one double poly bipolar transistor is a PNP transistor and wherein said at least one double poly MOS transistor is a PMOS transistor.

12. The semiconductor apparatus as set forth in Claim 7 wherein said at least one double poly bipolar transistor is an NPN transistor and wherein said at least one double poly MOS transistor is an NMOS transistor.

13. The semiconductor apparatus as set forth in Claim 7 wherein said at least one double poly bipolar transistor and said at least one double poly metal oxide semiconductor (MOS) transistor further comprise a second layer of polysilicon (Poly2) material wherein:

said second layer of polysilicon (Poly2) material in said at least one double poly bipolar transistor is doped with impurity ions to form an emitter; and

said second layer of polysilicon (Poly2) material in said at least one double poly MOS transistor is simultaneously doped with impurity ions to form an MOS source/drain.

14. The semiconductor apparatus as set forth in Claim 13 wherein said emitter in said at least one double poly bipolar transistor is self aligned to an extrinsic base of said at least one double poly bipolar transistor.

15. The semiconductor apparatus as set forth in Claim 13 wherein said MOS source/drain in said at least one double poly MOS transistor is self aligned to a gate of said at least one double poly MOS transistor.

16. The semiconductor apparatus as set forth in Claim 13 wherein said second layer of polysilicon (Poly2) material in said at least one double poly bipolar transistor is simultaneously doped with impurity ions to form a deep collector.

17. The semiconductor apparatus as set forth in Claim 13 wherein said MOS source/drain in said second layer of polysilicon (Poly2) material in said at least one double poly MOS transistor is etched to separate said MOS source/drain into a source and a drain.

18. The semiconductor apparatus as set forth in Claim 13 wherein said at least one double poly bipolar transistor is an NPN transistor and wherein said at least one double poly MOS transistor is an NMOS transistor.

19. The semiconductor apparatus as set forth in Claim 13 wherein said at least one double poly bipolar transistor is a PNP transistor and wherein said at least one double poly MOS transistor is a PMOS transistor.

20. The semiconductor apparatus as set forth in Claim 13 wherein said at least one double poly bipolar transistor is an NPN transistor and wherein said at least one double poly MOS transistor is a PMOS transistor.

21. The semiconductor apparatus as set forth in Claim 13 wherein said at least one double poly bipolar transistor is a PNP transistor and wherein said at least one double poly MOS transistor is an NMOS transistor.

22. A method for manufacturing a semiconductor apparatus comprising at least one double poly bipolar transistor and at least one double poly metal oxide semiconductor (MOS) transistor, said method comprising the steps of:

manufacturing said at least one double poly bipolar transistor in said semiconductor apparatus; and

simultaneously manufacturing said at least one double poly metal oxide semiconductor (MOS) transistor in said semiconductor apparatus.

23. The method as set forth in Claim 22 further comprising the steps of:

applying a first layer of polysilicon (Poly1) material to a substrate of said semiconductor apparatus;

doping said first layer of polysilicon (Poly1) material in said at least one double poly bipolar transistor with impurity ions to form an extrinsic base; and

simultaneously doping said first layer of polysilicon (Poly1) material in said at least one double poly MOS transistor with impurity ions to form an MOS transistor gate.

24. The method as set forth in Claim 23 wherein said at least one double poly bipolar transistor is a PNP transistor and wherein said at least one double poly MOS transistor is an NMOS transistor.

25. The method as set forth in Claim 23 wherein said at least one double poly bipolar transistor is an NPN transistor and wherein said at least one double poly MOS transistor is a PMOS transistor.

26. The method as set forth in Claim 23 wherein said at least one double poly bipolar transistor is a PNP transistor and wherein said at least one double poly MOS transistor is a PMOS transistor.

27. The method as set forth in Claim 23 wherein said at least one double poly bipolar transistor is an NPN transistor and wherein said at least one double poly MOS transistor is an NMOS transistor.

28. The method as set forth in Claim 23 further comprising the steps of:

implanting said substrate with impurity ions to form an intrinsic base in said at least one double poly bipolar transistor; and

simultaneously implanting said substrate with impurity ions to form a lightly doped drain in said at least one double poly MOS transistor.

29. The method as set forth in Claim 28 wherein said lightly doped drain in said at least one double poly MOS transistor is self aligned.

30. The method as set forth in Claim 28 wherein said at least one double poly bipolar transistor is a PNP transistor and wherein said at least one double poly MOS transistor is an NMOS transistor.

31. The method as set forth in Claim 28 wherein said at least one double poly bipolar transistor is an NPN transistor and wherein said at least one double poly MOS transistor is a PMOS transistor.

32. The method as set forth in Claim 28 wherein said at least one double poly bipolar transistor is a PNP transistor and wherein said at least one double poly MOS transistor is a PMOS transistor.

33. The method as set forth in Claim 28 wherein said at least one double poly bipolar transistor is an NPN transistor and wherein said at least one double poly MOS transistor is an NMOS transistor.

34. The method as set forth in Claim 28 further comprising the steps of:

applying a second layer of polysilicon (Poly2) material to said at least one double poly bipolar transistor and to said at least one double poly metal oxide semiconductor (MOS) transistor;

doping said second layer of polysilicon (Poly2) material in said at least one double poly bipolar transistor with impurity ions to form an emitter; and

simultaneously doping said second layer of polysilicon (Poly2) material in said at least one double poly metal oxide semiconductor (MOS) transistor with impurity ions to form an MOS source/drain.

35. The method as set forth in Claim 34 wherein said emitter in said at least one double poly bipolar transistor is self aligned to an extrinsic base of said at least one double poly bipolar transistor.

36. The method as set forth in Claim 34 wherein said MOS source/drain in said at least one double poly MOS transistor is self aligned to a gate of said at least one double poly MOS transistor.

37. The method as set forth in Claim 34 further comprising the step of:

simultaneously doping said second layer of polysilicon (Poly2) material in said at least one double poly bipolar transistor with impurity ions to form a deep collector.

38. The method as set forth in Claim 34 further comprising the step of:

etching said MOS source/drain in said second layer of polysilicon (Poly2) material in said at least one double poly MOS transistor to separate said MOS source/drain into a source and a drain.

39. The method as set forth in Claim 34 wherein said at least one double poly bipolar transistor is an NPN transistor and wherein said at least one double poly MOS transistor is an NMOS transistor.

40. The method as set forth in Claim 34 wherein said at least one double poly bipolar transistor is a PNP transistor and wherein said at least one double poly MOS transistor is a PMOS transistor.

41. The method as set forth in Claim 34 wherein said at least one double poly bipolar transistor is an NPN transistor and wherein said at least one double poly MOS transistor is a PMOS transistor.

42. The method as set forth in Claim 34 wherein said at least one double poly bipolar transistor is a PNP transistor and wherein said at least one double poly MOS transistor is an NMOS transistor.